



SINGLE BANK SDRAM TIMINGS

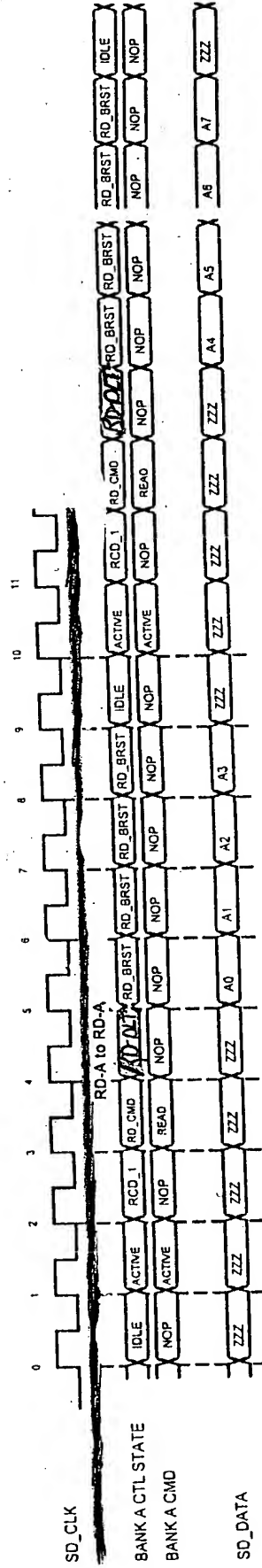


FIG. 15A

SINGLE BANK SDRAM TIMINGS

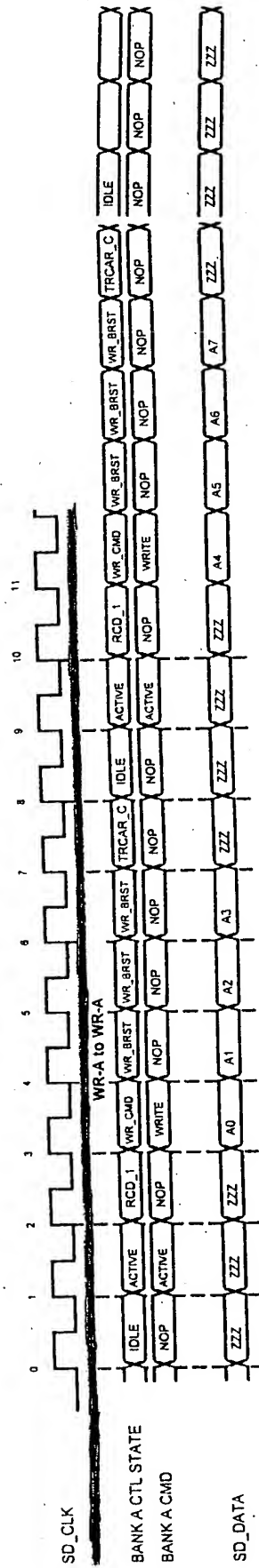


FIG. 13D

TWO BANK SDRAM TIMINGS

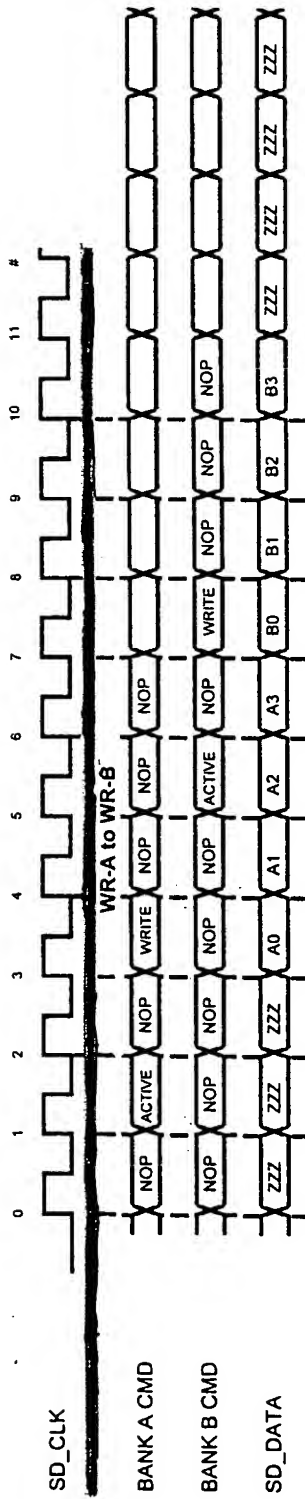


FIG. 16D